Minutes of Meeting report

Date: 22 March, 2025

Subject: Recap to basic analog elements & Verilog - AMS

**1. Agenda Items and Discussion:**

∙**Potential:** Discussion to electric potential, also known as voltage, which is the electric

potential energy per unit charge.

∙**Natures and Disciplines:** Disciplines are used to specify the type of a continuous wire

(ex: electrical, mechanical, rotational, optical, thermal, etc.). Natures are used to

describe the signals used in disciplines.

∙**Flow:** Discussion on the movement of electric charge, typically electrons, through a

conductor, creating an electric current. This flow is influenced by voltage (potential

difference) and resistance, with current flowing from a higher potential to a lower

potential.

∙**Discussion on RLC element and there working**.

∙**Forwarded** **Clock Architecture:**  reference clock signal from an external source is directly

passed through a transmitter to a receiver, ensuring the data and clock maintain a

consistent timing relationship during transmission and processing,

∙**CDR:** "CDR" most commonly stands for Clock Data Recovery, a circuit or function that

extracts the clock signal from an incoming data stream, enabling reliable data reception. 

∙**Current source:** a circuit element that delivers or absorbs a constant current, regardless

of the voltage across it, and is used to maintain a specific current flow in a circuit branch,

even when the load changes.

∙**Voltage Source:** a device that provides a potential difference (voltage) between two

points, enabling current flow in a circuit, with common examples including batteries and

generators.

∙**Resonance Frequency :**the specific frequency at which a circuit, particularly an RLC

(resistor, inductor, capacitor) circuit, exhibits a maximum oscillatory response or

impedance change, where inductive and capacitive reactances cancel each other out**.**

 ∙**Quality Factor :** the quality factor (Q factor) is a dimensionless parameter that measures

the sharpness of resonance or the energy storage capability of a resonant circuit, with a

higher Q factor indicating a sharper resonance and less energy loss.

∙**Active & Passive component :**How to state the current direction in both.

2. **Coding of component**

**∙Voltage Amplifier**

**∙Current Control Current Source**

**∙Voltage Control Voltage Source**

**∙Current Mirror**

**∙Resistor , Capacitor & Inductor**

2.**Assignments:**

∙**LTSpice Circuit Design and Simulation:**

          Anas, Govind - LDO

         Rohini, Mahendra, Pushpak - ADC

          Sanika, Srujan - GPIO

         Shrishti, Kedar - Buffer

          Nakshatra, Gururam – Amplifier

 ∙**To Create models of above assignment**.

**Minutes of Meeting report**

Date: 15 March 2025

Subject: Introduction to Analog Mixed-Signal (AMS) Design and Verification

**1. Agenda Items and Discussion:**

* **Chip Architecture:** Discussion on chip architectures and blocks such as LDO, GPIO, etc.
* **Radio Frequency Integrated Circuits:** Overview of RFIC structures and internal blocks, including antennas, Low Noise Amplifiers, mixers, balancers, and MEMS, Waveguides, and Microwaves
* **Frequency Modulation vs. Amplitude Modulation:** Discussion on why FM is used for short distance and AM for long distance signal transmission. Discussion on Difference in power consumption between transmitting FM and AM signals.
* Discussion on why **TV stations utilize large-diameter cables** for signal transmission.
* **Op-Amps:** Discussion of Op-Amp specifications, the Fourier and Nyquist theorem, and their applications in Op-Amp circuit design.
* **Audio and Video Signals and Amplifiers:** Overview of audio and video signal characteristics and the design of corresponding amplifiers.
* **Chip Design Flow Overview:** General overview of the chip design flow, from specification to fabrication.
* **Architect Role and Block Division:** Discussion of the chip architect's role and the process of dividing design blocks among different departments.
* **High-Resolution Simulation and IBIS Models:** Explanation of why high-resolution simulations take long time and how Input/Output Buffer Information Specification (IBIS) models can be used to reduce simulation time.
* **EDA Tool:** Explanation of how EDA tools convert design parameters into mathematical equations for simulation.
* **RTL Models and GPIO Testing:** Discussion of how Register-Transfer Level (RTL) models can reduce simulation time and facilitate GPIO block testing across various bandwidths.
* **Need and Role of AMS:** Discussion on the necessity and role of Analog Mixed-Signal (AMS) design in modern integrated circuits.
* **AMS Verification:** Discussion on Co-simulation and how the main role of AMS verification engineer is to create models and conduct cosimulations.

2. **Assignments:**

* **LTSpice Circuit Design and Simulation:**

          Anas, Govind - LDO

          Rohini, Mahendra, Pushpak - ADC

           Sanika, Srujan - GPIO

          Shrishti, Kedar - Buffer

           Nakshatra, Gururam – Amplifier

* **To create a ppt** on the need for AMS, AMS understanding, and modeling techniques.

**Minutes of Meeting report**

Date: 29th March 2025

Subject: Revision of UVM concepts and Introduction to AMS Flow

* 1. **Agenda Items and Discussion:**
* **Basic revision and introduction to UVM methodology:** Discussed analogy between daily life with concepts like randomization, etc.
* Discussion of SV concepts like semaphores, mailbox, and assertions.
* Revisited testbench functionalities and discussion on: directed vs constrained randomization test (with an example of ADC).
* Overview of Coverage Convergence life cycle.
* Definition of Seeding. Along with an example of a DAC.
* Why is there a need for randomization? Use of rand and randc. Discussed with an example of sudden temperature change in a system.
* **SV Testbench Architecture in terms of levels:** Signal Level (DUT), Command Level (Driver, Assertions, Monitor), Functional Level (Agent, Scoreboard, Checker), Scenario Level (Generator). All inside of an environment.
* **Datatypes:** Why use two-state datatypes over integer? (think in terms of memory usage). Then more discussion on built-in datatypes, especially *wire vs reg vs real.*
* **Arrays:** Types of arrays, packed vs unpacked arrays, and choosing which one to use and when.
* **Timevalues:**time-unit/time-precision and using **`***timescale* compiler directive
* **OOPs:** Example snippet of a CRC (Cyclic Redundancy Check, an error-detecting code consisting of XOR operations).
* Discussion on static vs global variables, routines (task & function, scoping rules like name-scope)
* Using one class inside another class using object handler, Copying and modifying objects. Types of copying methods: Deep and Shallow copy
* Use of Arbiter in Testbench and a simple use case
* Use of Interface: Communication between ports, use of *modport* (example of HDMI cable connection with laptop)
* **Threads and IPC (interprocess communication):** Overview of the following: Fork and join, semaphores and mailbox, Events, assertions (Assertions vs Constraint), Factory Patterns, Sequences, Covergroups.
* **AMSD Use Models:** With an example of SERDES. The SERDES contain at least 20 analog standard cells and how to verify them together with the Digital VLSI system. Simulation results of Duty Cycle Correction (DCC) analysis were shown.
* **Expanded on Mixed-signal Flow**: Addition of Analog Spice circuit and Analog cell checkers in the RTL Validation Testbench

2. **Assignments:**

Project Teams:

* 1. Anas, Mahendra, Srishti
  2. Govind, Nakshatra, Sanika, Srujan
  3. Pushpak, Kedar, Rohini, Gururam

**1st assignment:** Make a presentation of at least 15-20 slides from ***Verilog-AMS LRM*** based on assigned chapters.

Chapter 1,2: Everyone

Chapter 3, 6, 8: Team (Anas, Mahendra, Srishti)

Chapter 4, 7, 10: Team (Govind, Nakshatra, Sanika, Srujan)

Chapter 5, 9, 11: Team (Pushpak, Kedar, Rohini, Gururam)

**2nd assignment**: Read and solve practice problems from Razavi’s Analog IC book till Ch.5